3D CHIP SCALE PACKAGE (CSP)

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Increased Density Approaches

Package/die stacking technology enhances most aspects of electronic systems such as size, weight, speed, yield, and power consumption. Their reliability and robustness could also be improved if the faulty package/die is systematically eliminated during the stacking assembly. Currently, stacking is limited by a number of factors. Some of the limitations such as thermal management, stem from densification, others are due to the current technological limitations, such as via diameter, line width, via pitch, and line spacing. It is expected that the effect of such limitations will decrease as the packaging technology advances.

The main issues in stacking are quality and density of the inter-stacking interconnects, electrical, mechanical and thermal characteristics, design tool accessibility, reliability, testability, rework, special set up and package cost, known good die (KGD), and fabrication time. These factors determine the selection of a stacking technology for an application. Since most stackings are designed for special applications, they lack standardization as well as information accessibility generated by the stack manufacturers. These issues have been resolved for the cases where standard packages are stacked.

Two approaches have been used to increase electronics density, i.e., the total memory capacity available divided by the space occupied on PWB (printed wiring board). Density increases have been achieved by the following techniques:

- Increasing density of memory chip and packaging. The chip scale packaging (CSP) approach is an example of size reduction through package shrinkage without increase in the memory chip density. Size reduction in memory chip has been achieved through advancement of photolithography technology and use of new materials and techniques enabling finer feature die circuitry.
- Stacking memory/packages on the board using the standard technology. Stacking bare chips and multichip modules (MCM) normal to the board can increase the memory density without sacrificing the board space. Stacking based on MCM technology has been widely adopted for increases in density. Similar approaches are being adopted by many manufacturers using TSOP (thin small outline package) and CSPs to further increase density.

This chapter will review different stacking technologies: bare die, multichip module, and the most recent development for CSP stacking. Examples of peripheral and grid CSP stacks are discussed in detail.

Review of 3D Stacking

Previously, aerospace and military applications were the key demands for higher density electronics packaging in order to meet the stringent requirements for weight reduction. Now, this trend has become more common for commercial portable electronics with significant demands for low power, low weight, and compact packaging. In order to meet these demands, many new stack packaging technologies have emerged duplicating those developed for the MCMs, i.e., by stacking along the height for saving space on board. The stacking technology also results in a much lower overall interconnection length and parasitic capacitance, resulting in reduced system power consumption.

3D interconnection generally refers to the interconnections needed to route power, ground, and signals to the layers within the stacking configurations. Even though it is difficult to distinguish their differences in many stacking configurations, here, they are categorized into three types to better understand similarities to previous and newly developed stacking technologies. The three categories include stacking of bare dies, MCM, and CSPs with interconnection of either peripheral or area array. Area array technology can accommodate much higher number of interconnections for the base stack and therefore for the 3D stacking. The three main categories are briefly discussed in the following. Refer to Al-Sarawi et al [1], for a more in depth review of the status of bare die and MCM technology.

Bare Die

- Peripheral
  - Direct contact between the die and PWB (printed wiring board). Connection can be accomplished by TAB (tape automated bonding) or solder balls. Connection to PWB is either by peripheral or area array.
  - Die are connected through an the edge conductor and then attached to the PWB. The conductor can be a separate entity or part of the stacking. Attachment to conductors can be accomplished by TAB, solder filled via, conductive adhesive, or thin film contact. Connection on the die face accomplished by sputtered metal conductors, or direct laser write traces on an epoxy cube. Conductor connection to PWB could be peripheral or area array.
- Area Array
  - Flip chip bonded stack with and without spacer. Dies are flip chip and bonded to either a substrate or another die and a spacer could be used to control the gap between the stacks. Microbridge springs have also been used for the stack interconnection.
  - Stacked silicon wafers with filled vias: In this method, vertical interconnections are formed using vias etched through the entire wafer and then filled with metal. The bottom side of the filled via contacts the top surface of a metal pad on the adjoining wafer. The filled vias are connected by applying pressure on the stack. This method was developed and used by Micron Technology for high density data storage using stacked non diced wafers.

MCM

- Peripheral

- There are many similarities in interconnect technology for MCM and Bare die. Generally, differences exist on those aspects which are unique to either technology. For example, direct use of wire bond is only possible through MCM-D, or the use of solder dip for the stack interconnect. An elastomeric interconnection version of this technology was evaluated by the Jet Propulsion Laboratory (JPL) for space application in the New Millennium Program (NMP) [2]. The horizontal mount cube (HMC) version was recently considered for the X-2000 of NMP [3].
- Area Array- This aspect of technology provides much higher density and has progressed rapidly in recent years. Examples are shown below:
  - Fuzz buttons as stacking interconnect MCM as well as clearance for chip and bond. This layer has a precision plastic spacer to provide clearance for chip and bond, and fuzz buttons to provide interconnection by applying a mating force on the stacked MCMs. Fuzz buttons are physically made of fine gold with good interconnect integrity.
  - Elastomeric connectors with electrical feed throughs: The vertical interconnections in this method are implemented by a combination of "electrical feed throughs" and elastomeric connectors.

CSP

Direct stacking of bare memory chip can be costly and there are several issues that are yet to be resolved. These issues are similar to those issues when CSPs were compared to bare die. For example, lack of known good die, difficulty in handling, testability, and high assembly cost are a few. Nevertheless, this approach has been adapted by NEC using area array with interposer, and Fujitsu with die stacking and followed by packaging in CSP.

In the stack package technology, several packages of the same kind such as TSOP, SOJ (small outline J-lead), and a mixture with CSP are stacked in a vertical direction. The following CSP stack technology will be discussed.

- Peripheral
  - Conventional TSOP, SOJ, and SOC (small outline C-lead) are stacked in the vertical direction. Bare die stacking in conventional package.
  - CSPs of the same types are stacked or a mixture of CSP and conventional leaded packages are stacked.
- Area Array
  - Chip Scale package.
  - Flip chip bare die are stacked and then stacks interconnected by peripheral solder bumps.
  - Bare die are stacked internally with wire bond and then packaged in a grid CSP.
  - CSPs are stacked with the stacks interconnections by peripheral solder bumps.

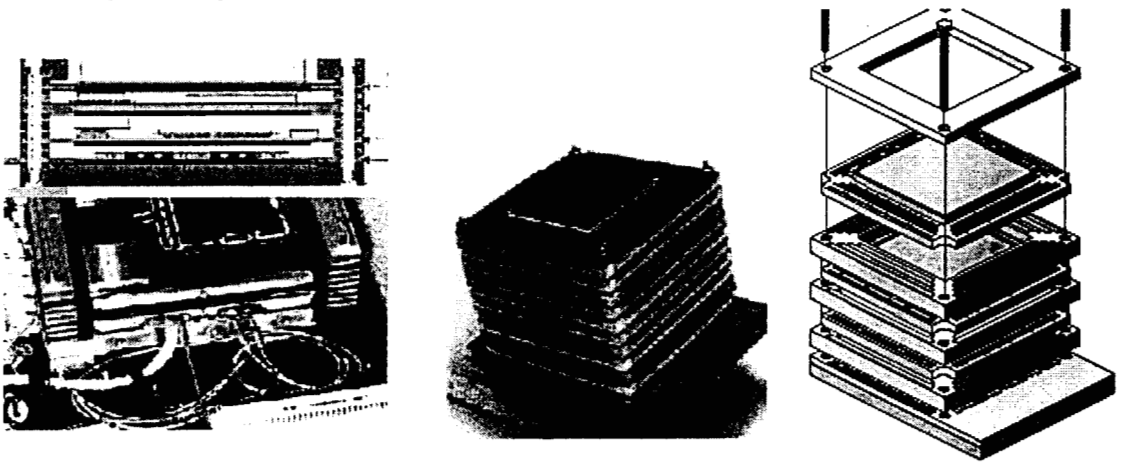
CSP is an emerging technology with significant potential growth in stacking. Many of the stacking techniques for conventional packages could be implemented for CSP once materials, process, and system development for finer features are developed.

After a brief review of MCM for space applications, the CSP stack technology from the following suppliers will be discussed:

- Staktek [4] which uses stacking of conventional SOJ and TSOP packages
- Samsung Electronics [5] which uses stacking of conventional SOJ
- Fujitsu [6,7] which uses conventional SOC lead package and memory stacks in a grid CSP
- Hyundai [8] which uses stack chips packaged in a conventional SOJ package
- LG Semicon [9] which stack their BLP (bottom leaded package) leadless package [10] on the top of a conventional small outline L-lead package (SOL)
- NEC [11,12] which uses flip chips on substrates which are stacked through peripheral solder bumps
- Micron Technology [13] which uses an area array stack design

3D MCM For Aerospace Applications

Recent changes within NASA's exploration program favor the design, implementation, and operation of low-cost, light weight, small and micro-sized spacecraft, with multiple launches per year rather than several missions per decade. To meet the current and future needs of NASA's JPL, the 3D stacking technology (including 3D chip stacking, horizontal and vertical space cube MCM stacking) have been investigated. Figure 1 shows the trend for the 3D packaging architecture which was validated under the Advanced Flight Computer (AFC) for the NASA's New Millennium Program (NMP).



New Millennium
DS-1
320 I/O
PWB Technology
4.0" x 5.8"

2nd Generation
Micro-Spacecraft
640 I/O
PWB Technology
3.7" x 3.7"

Next Generation
Space Cube
800 I/O
MCM Technology
3.5" x 3.5"

Figure 1

Figure 1 3D MCM for space applications

The qualification tests on the AFC 3D MCM included vibration, thermal vacuum, thermal cycling, and accelerated aging. This technology was an important development step towards further integration of avionics for the NASA's Deep Space System Development Program [2].

The vertical space cube is one of the next generation of 3D stack which builds on:

- Stacking MCM Packages

- Elastomeric Interconnects
- 200 I/O on each side of the stack, 3.5 by 3.5 inch package
- Double sided package

The most recent 3D MCM is the horizontal mount cube which was validated under the outer planet technology (X2000) of NMP [3]. The X2000 objectives are to advance the state of the art in spacecraft system development every three years with its first engineering model delivery by the year 2000, hence X-2000. Two of NMP's missions are the ST4/Champollion - a Comet Lander, and a Europa Orbiter. These missions incorporate the X2000 avionics architecture with a low cost system. The architecture will integrate different instruments, propulsion modules, power sources and telecommunication for multiple missions. The goal is to develop a modular building block design with standard interfaces enabling a high level of system integration. System on a chip (SOC) is the next generation of the integrated system.

Specifically, the HMC houses command and data handling as well as power and altitude control electronics. Figure 2 shows the interstack (z-horizontal interconnection) with each slice of 4.0 inch^2 x 0.5 inch aluminum frame. The HMC improves subsystem interchangeability and size scaling through the vertical configuration, along with improved dynamic and thermal characteristics.

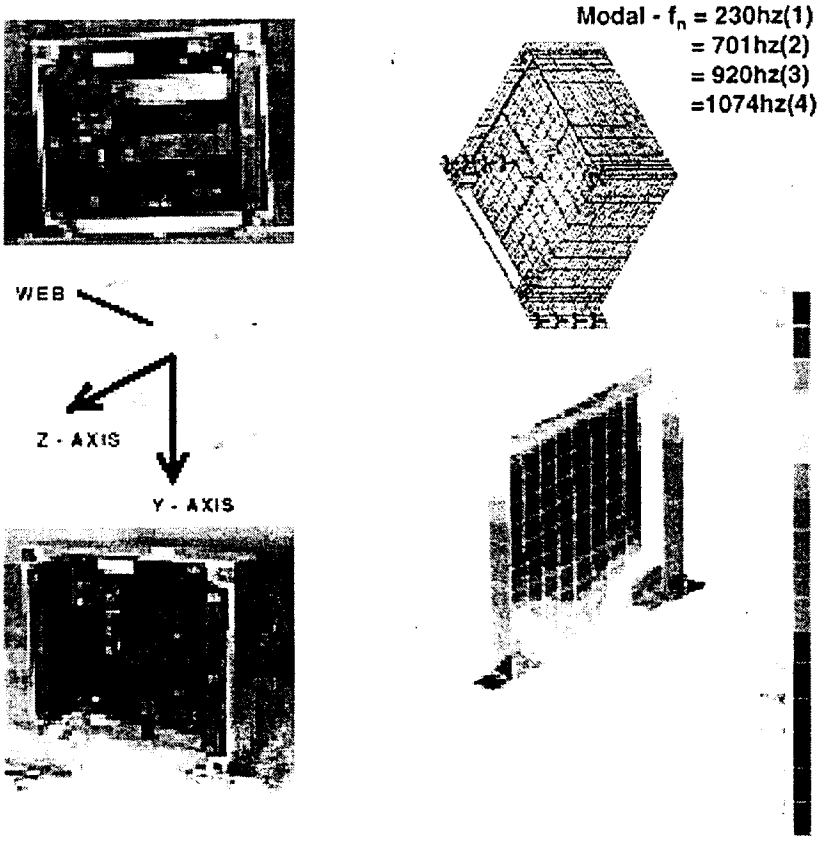


Figure 2 Horizontal Mount Cube (HMC) MCM and Temperature Distribution

Dynamics and thermal tests were performed to determine package integrity, thermal dissipation characteristics, and electrical signal integrity under a simulated flight extreme operation condition. The dynamic test included in situ testing of the y and z-axis connectors. Eight circuit paths threaded through over 11,000 pin contacts covering 91% of the total I/Os in the system. The IAS (integrated avionics system) was instrumented to detect open pulses within 11ns. The primary testing was high-level random vibration, augmented by low-level sine sweep for model correlation and detection of changes in response along with simulated pyrotechnic shock.

A thermal vacuum test was performed over a 3-day period on a prototype panel with mounted HMC, with the following objectives:

- Verify electrical continuity of the Y- and Z-axis connectors during three qualification cycles in the range of -70°C to +75°C.
- Determine the thermal performance by measuring the panel temperatures at nominal and high power.

The thermal performance of the 3D stack and the IAS panel in the test agreed fairly closely with thermal analysis projections. The analytical thermal model predicted the actual slice interface temperature within 10°C in the nominal power case, and within 1°C in the high power case. Adjusting the longeron-to-panel thermal conductance in the model was expected to improve model predictions. The maximum temperature rise from the slice interface to the middle of the flight computer PWB in the high power case (for a slice dissipation of 8.0W and a stack dissipation of 57W) was 20°C. The maximum flight computer PWB temperature in this case was 43°C. The 3D stack and the IAS panel have been proven to efficiently dissipate heat to an external environment sink.

In summary, the dynamic and thermal environmental tests validated that the HMC packaging design meets or exceeds performance projections. The in situ dynamics test results indicated no opens during test, and the thermal vacuum test showed that the 3D HMC stack and IAS design efficiently dissipate heat to an external environment.

STAKPAK™

Figure 3 shows this approach for increased in memory capacity. It utilizes the standard TSOP packaged parts to increase memory without increasing board space. The density increases are in 2X (double) and 4X configurations which all fit in the same space as 1x density and are electrically compatible with the system memory bus. This means that a 4X stacked SIMM will reduce motherboard space and the number of SIMM sockets by a factor of four over a conventional SOJ SIMM.

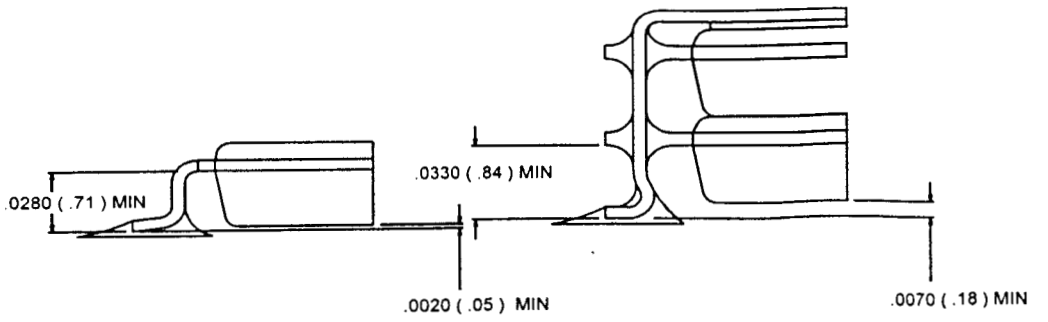


Figure 3 Comparison of cross sectional view of TSOP and Stakpak™ Technology

The Uniframe Stakpack™ uses a copper lead alloy interconnect system that provides a structure and an efficient electrical and thermal path for standard TSOP package DRAMs in a 3D configuration. The build up details for this and Flexfram™ are shown in Figure 4. The stack can be easily tested, reworked, and are compatabile with industry standard surface mount equipment and processes. The θj for the two stack configurations to TSOP is shown in Figure 5.

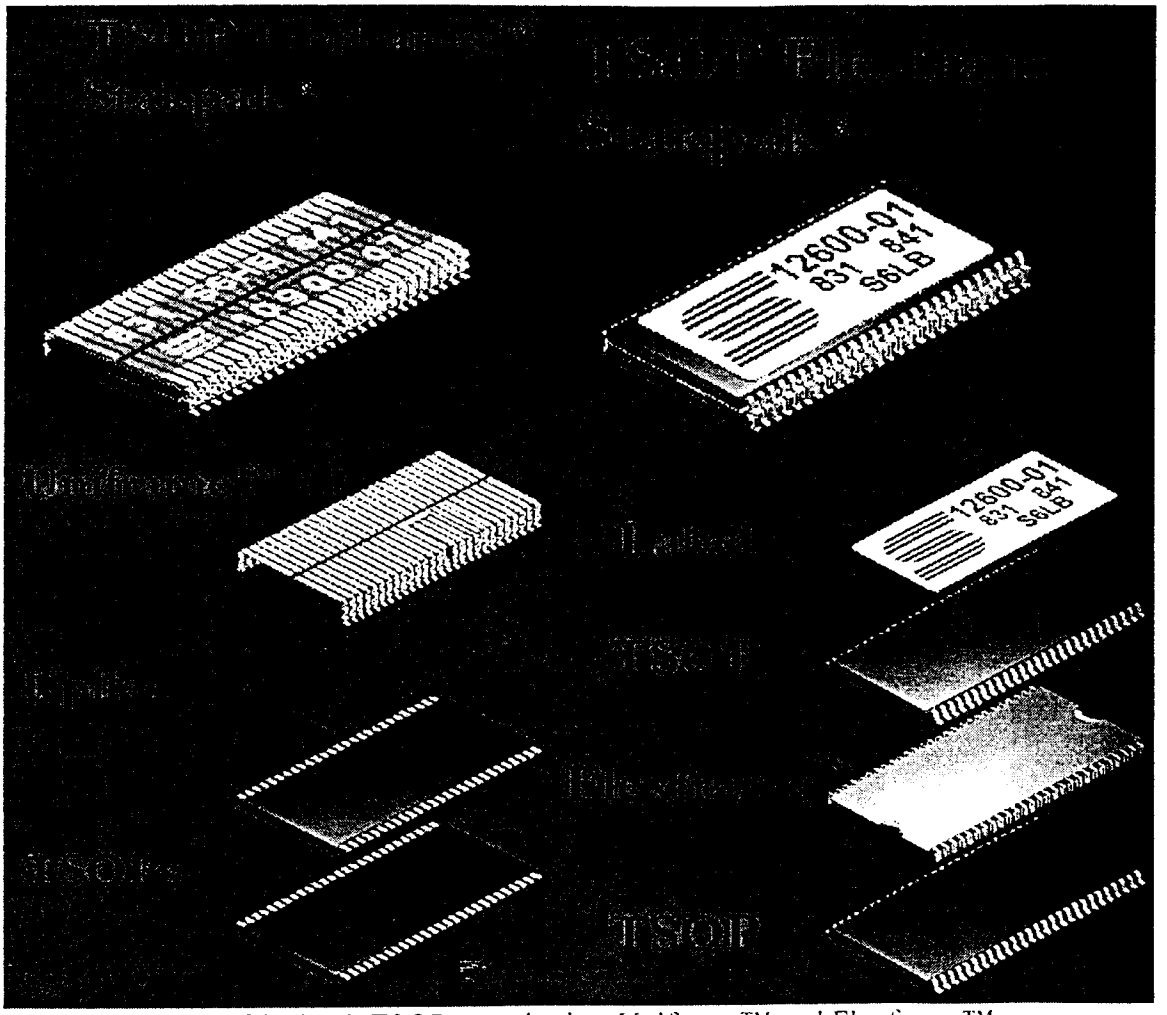


Figure 4 Two types of Stakpak TSOP tecnologies. Uniframe™ and Flexframe™

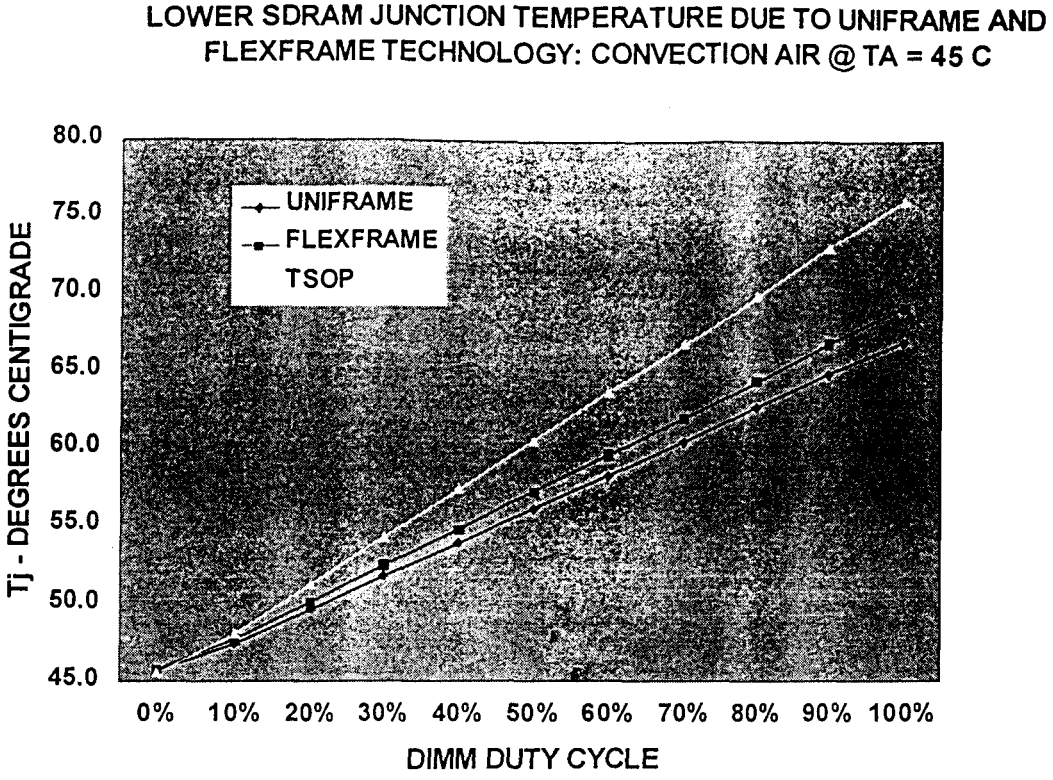


Figure 5 Lower SDRAM junction temperatures for the TSOP, Flexframe, and Uniframe

SAMSUNG 3D MEMORY

The Samsung 3D memory module technique utilizes conventional thin quad flat J-lead (TQFJ) for stacking. The number of stacks in a memory module depends on the memory density requirement. Figure 6 compares the stack package size with its conventional leaded package. Since the stack uses a conventional package, no changes are required for the PWB foot print design. Manufacturing processes are also well known. The stack is shown to have improved reliability, but degraded thermal dissipation characteristics compared to its package [5]. It was shown that the maximum junction temperature was higher for the stack than the discrete package which increased linearly with power. Tables 1 and 2 list package and stack reliability. The stack package passed the following environmental exposures:

- Humidity exposure, 85°C/65% RH, 1,000 hours
- Pressure cooker test (PCT), 121°C, 2 atmosphere, 240 hours
- Temperature cycle test (-65°C to 155°C, 1,000 cycles)

The stack assembly showed no failures to 1,000 thermal cycles in the range of 0 to 125 °C.

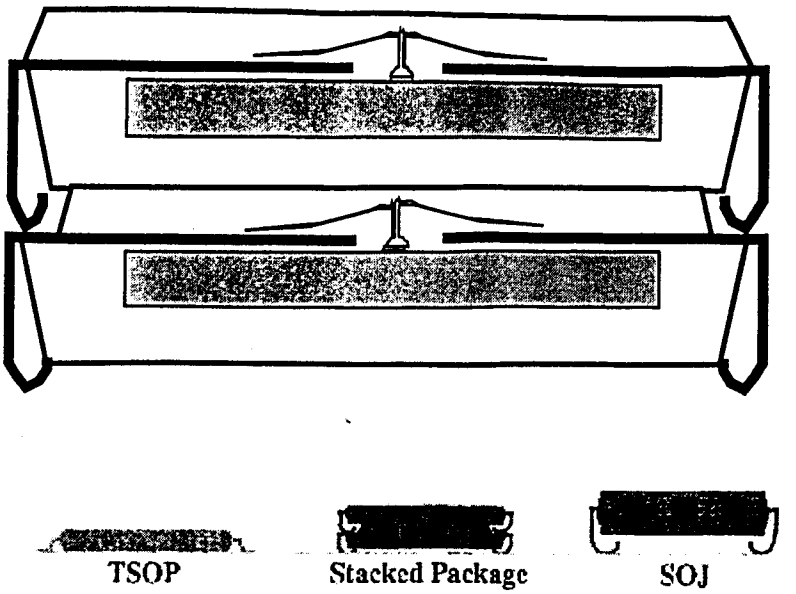


Figure 6 Samson 3D Stack memory and size comparison to conventional package

Table 1 Unit and stack module environmental test data

Temp / Pkg.	85°C/65% (168 hrs)	Temp. Cycle (-65 to155 °C)	IR. Reflow (235 °C)	Remark
Top Package	0/116			
Bottom Package	0/116			
Stacked Package with PCB	0/10 Modules (Visual Inspection)			-32EA Stacked Package Mount

Table 2 Stack temperature cycle data

Cycle / S/J		300 cycles	600 cycles	1000 cycles	Remark
Solder Joint (0 to125°C	Dummy Stack	0/116	0/116	0/116	32TSOJ Stack

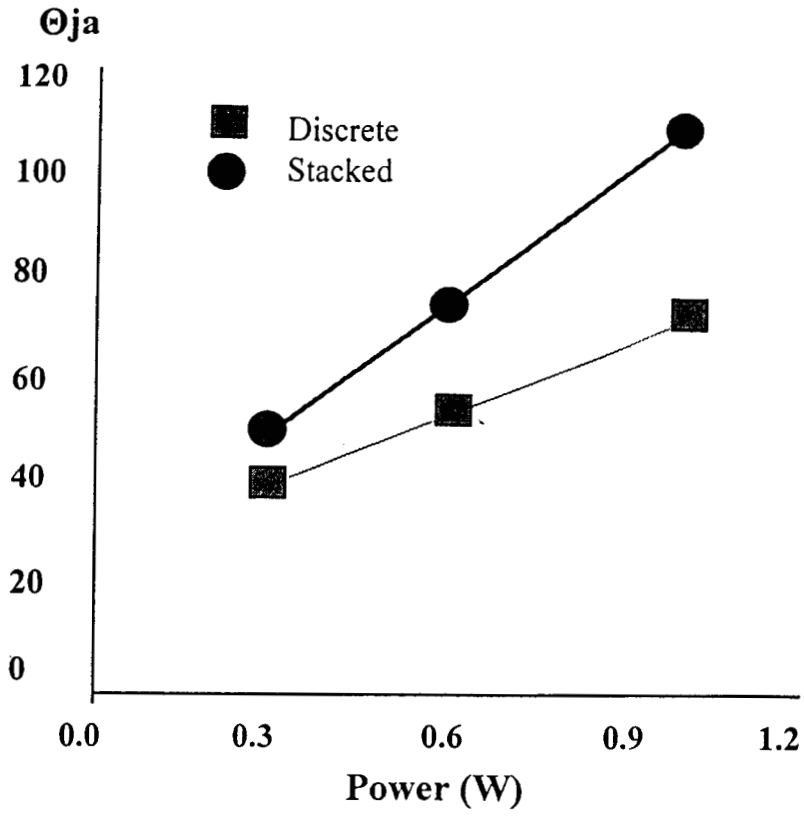


Figure 7Thermal dissipation comparison of discrete and stack configurations

Fujitsu

Fujitsu developed a small outline no-lead (SON) package which later it evolved to be the small outline C-lead (C-lead). Both packages are peripheral and aimed for low pin counts (<50) such as memory devices. The C-lead, similarly to the TSOP stack package, was stacked to form a three-dimensional packaging module (3DPM) as shown in Figure 8.

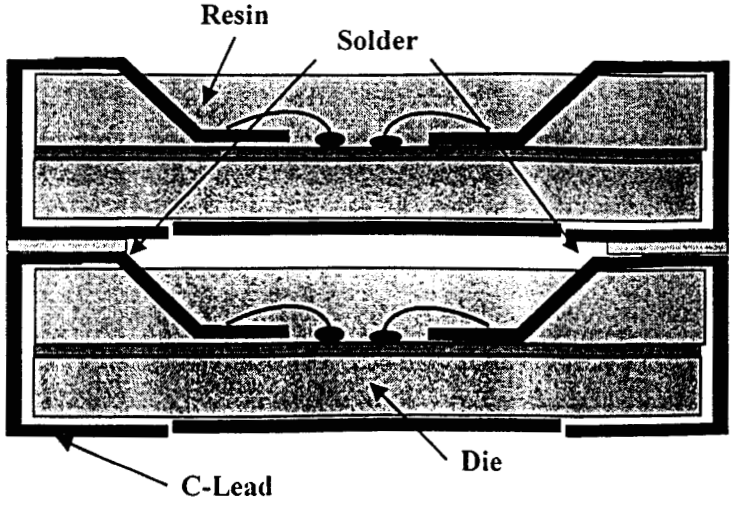


Figure 8 Fujitsu's three dimensional packaging module

Electrical simulation modeling showed that SON and SOC have better electrical performance than a conventional TSOP. The improvement was attributed to their shorter height and length than TSOP. Thermal performance for SON is also better than TSOP. This is not true for SOC and TSOP. In either case, the copper lead configuration has better thermal characteristics. The four stack (Figure 9) showed the best performance both for Cu and alloy 42.

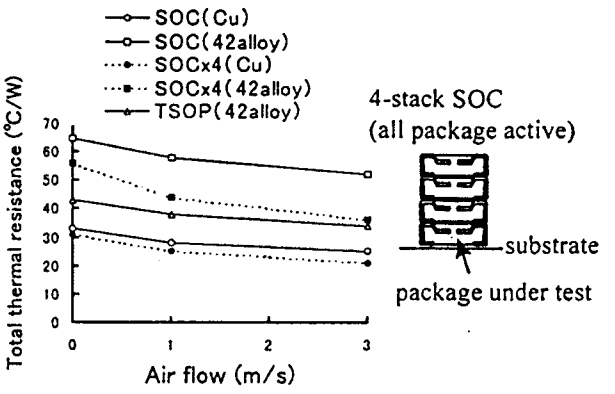


Figure 9 Thermal performance of TSOP and SOC , and 3D SOC with Alloy 42 and copper leads

The SOC single packages were subjected to thermal cycling and the pressure cooker (PCT) test. It passed 1,000 thermal cycles in the range of –65°C to 150°C and 168 hours of PCT at 121°C and 85% relative humidity. In addition the solder joint thermal cycling behavior of the SOC 3D packages on FR-4 were compared to its single SOC package and TSOP on a double sided PWB. Table 3 lists cycles to failures for these packages. All packages passed 500 thermal cycles in the range of –55 to 125°C with the least damage (cracks) for the SOC stack version [6].

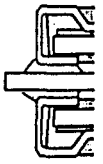
		100	200	300	400	500
TSOP50 (n=20pcs)	crack	OK	OK	3/20	6/20	13/20
	open	OK	OK	OK	OK	OK
SOC46 (n=30pcs)	crack	OK	OK	OK	OK	5/30
	open	OK	OK	OK	OK	OK
3DPM(×2) (n=10pcs)	crack	OK	OK	OK	OK	1/10
	open	OK	OK	OK	OK	OK

Double-sided (symmetric)

T/C condition : -55℃~125℃

PKG : SOC-46 /TSOP-50

Board : FR-4 (84mm × 74mm × 0.5mm)



substrate

Table 3 Thermal cycling behavior of 3D SOC compare to single SOC and TSOP on FR-4

Stack Chip Package (SCP) by Hyundai

In an attempt to provide a high density memory solution, especially for workstation and PC servers, a multichip package (stack chip package) has been developed. The major characteristics are as follows: (1) SCP contains a plurality of both memory chips and lead frames serving as an interposer within a molded plastic package, (2) chip selection is made through the wire bonding option. Each chip is selected alternately, resulting in the package with a memory capacity twice or four times that of a monolithic chip. (3) plural lead frames are electrically interconnected all at once, using metal solders electroplated on the lead frame surface, (4) SCP was found to be reliable and cost competitive when compared to other stack packages because it basically adopts the molded plastic packaging technology as well as the metal solder interconnection method.

SCP Design

Figure 10 shows the cross-sectional drawing of a two dimensional SCP. The two memory chips in mirror images are bonded through leadless and leaded frame with solder as interposer. Basically the stack chip package contains two types of lead frame with 6 mil (0.1524 mm) cavity depth at the chip center. The depth is determined such away as to avoid contact between the top and bottom chip gold wires. Electrical interconnection between the two lead frames are formed by solder, a low cost joining technology. Other two dimensional versions are:

- A face up and a face down chip
- A face up and face up chip
- A face down and a face down chip

- A face up and face down with peripheral boundary (see Figure 10)

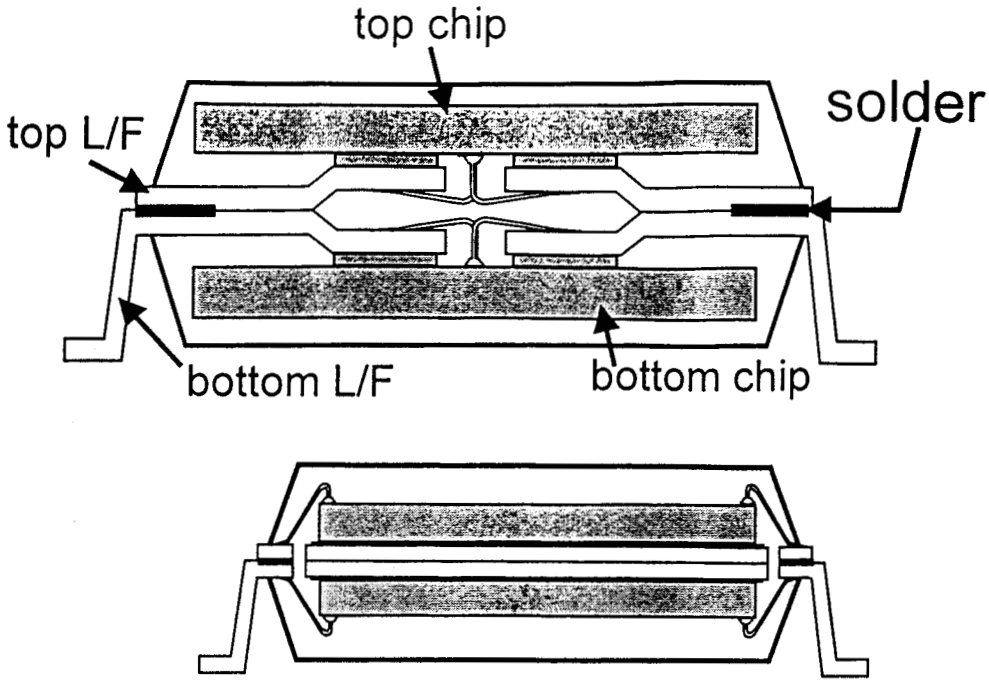


Figure 10 Two stacks of a face up and a face down chip (top drawing) and a peripheral chip bond

Figure 11 shows an assembled SCP. The SCP also fit in the SOP (small outline package) package category since it has similar dimensions, i.e. 380 mils (9.652 mm) and 875mils (22.225 mm). SCP, however, has no specific limitations to the package format, package external size, and the kind of DRAM chips stacked.

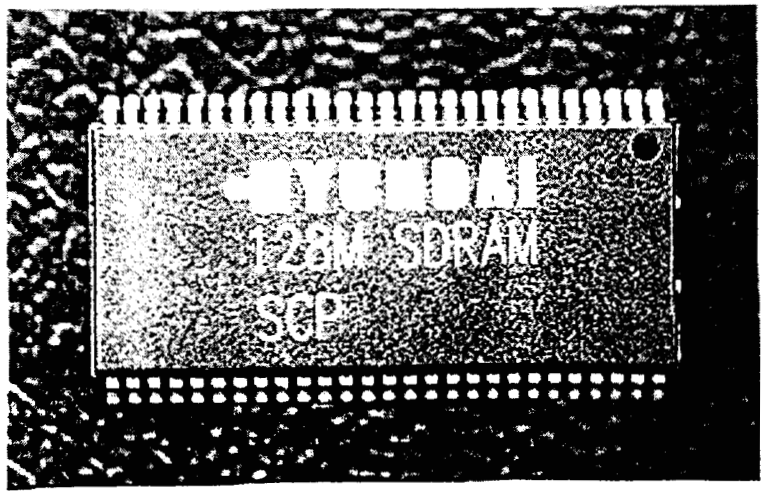


Figure 11 Assembled SCP

An example four dimensional SCP is shown in Figure 12. This package has two stacks of two face-down chips and two face-up chips. Other variations include: (1) two stacks of a face-up and a face-up chip, (2) two stacks of two face-up and two face-down chips, and (3) a chip with peripheral I/O pads.

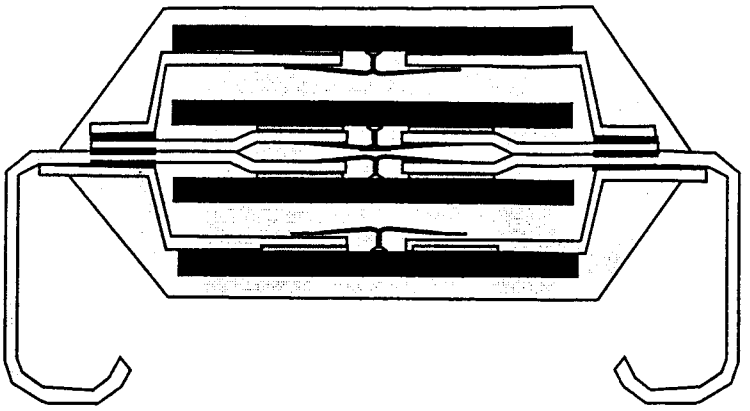


Figure 12 Four dimensional SCP stack, two stacks of two face down and two face up chips

Table 4 compares thickness and reliability of a two dimensional chip stack to a two dimensional package stack. Chips stacked in a package are expected to show comparable reliability to the conventional plastic package such as TSOP. In contrast, reliability of stack package is expected to be inferior to TSOP since it requires additional solder joints.

Table 4 Comparisons of Hyundai's 2D SCP and 2D TSOP package technology.

Items	2D chip stack	2D package stack
Feature	One SOP	Two TSOPs
Package Thickness	About 1.8mm	About 2.2mm
Reliability	Comparable to TSOP	NA

Assembly

Electrical interconnection between top and bottom chips can be accomplished by various methods. These include:

- Laser welding
- Conductive epoxy
- Solder

Joints also should have adequate strength to guarantee stable electrical interconnection between top and bottom lead frame during assembly and in field.

Laser welding was considered by Hitachi [14]. Except for the laser, other bonding technologies generally require a medium to electrically and mechanically join two components together. The most common bonding media in electronic applications are solder and electrically conductive polymeric

adhesive materials. Joint materials provide electrical, mechanical, and thermal conduction path between the two components. Solder is preferred where high electrical and thermal conduction is required.

The room temperature volume resistivity for several solder materials and conductive polymer adhesives is summarized in Table 5. The resistivity for the silver-filled epoxy, a conductive polymer, is an order of magnitude greater than solder. The high resistivity of conductive polymers have impeded their widespread use compared to solder materials. In addition, silver-filled epoxy needs post cure, an additional thermal process step and a further delicate handling requirement of soft adhesive to avoid damage before thermal cure exposure. Because of these shortcomings, the silver-filled epoxy was not considered for bonding evaluation.

Table 5 Electrical volume resistivity of several solder materials and silver-filled conductive adhesive at room temperature.

Materials	Sn	Ag	Sn-37Pb	Sn-0.7Cu	Sn-3.5Ag	Ag-filled epoxy (filler content=82wt%)
Resistivity ($\times 10^{-6}\Omega$cm)	10.9	1.6	15.0	12.9	7.5	80

The following criteria were considered to narrow selection of solder materials for the SCP lead joining:

- Solder with no requirement for flux. Flux cannot be used during joining because its residues need to be cleaned before transfer molding. Cleaning is impossible since the bare chip gold wires are exposed and can be contaminated. To avoid a required control of chemical composition, pure metal was chosen for the lead surface finish.
- Solder with low risk to environmental pollution
- Solder with low electrical resistivity
- Solder with low materials and process cost
- Solder with adequate joint strength
- Solder with low alpha particle emission since it applied near bare die
- Solder with potential long term availability

It is known that memory chips are very sensitive to radioactive alpha particles emitted from lead (Pb), and this results in device malfunction. Therefore, a lead (Pb) free solders is strongly recommended as a bonding medium.

The joining method depends on lead frame surface finish. Two candidates were selected for in depth investigation: (1) fluxless Ag/Sn and (2) high-pressure mechanical joining of silver.

Fluxless soldering joint of Ag/Sn

For the fluxless soldering joint of Ag/Sn, the two lead surfaces were selectively electroplated with 5 μm-thick silver and 5 μm thick tin sequentially. During the joining process, the two lead surfaces were brought into contact under static pressure and heated in nitrogen above the tin melting temperature, i.e., 232°C. Nitrogen gas was used to prevent the tin layer from oxidation, in order to achieve a high quality

joint. Micro sectioning plus SEM EDX analyses indicated that the Ag/Sn fluxless joint introduces a multilayer structure of $Ag/Ag_3Sn/Sn/Ag_3Sn/Ag$/on the lead frame.

High-pressure mechanical joining of silver

Since the silver melting temperature is too high to be applied as a fluxless solders, elevated temperature, high pressure mechanical joining was required. A process temperature as high as 200°C was needed to achieve a high strength joint. The joint surfaces were electroplated with 7μm -thick silver to ease bond formation. Joining was accomplished by application of static pressures ranging from 10 kN to 60 kN at elevated temperature. Unlike the fluxless soldering, no nitrogen atmosphere control was required.

The mechanical joints resulted in a nearly constant bondline thickness whereas the fluxless joints showed variation in thickness due to tin melting during joining. Feasibility of Ag/Sn plating for high-pressure mechanical joints was also studied, though results are not presented here. It was demonstrated that molding pressure applied at 175°C during the package process is sufficient to achieve a strong bond. This means that the initial process step for mechanical joining can be eliminated; reducing the cost.

Mechanical strength of lead-to-lead joint

Solder joint integrity was determined by a lap shear test designed for this purpose as shown in Figure 13. The joint area was 0.4536 cm^2. Four samples were tested for each joining system. Figure 13 also shows the average shear strength test results for two joint materials. The joint strength for high-pressure mechanical silver joint with 49.1 MPa was higher than 32.7 MPa for fluxless Ag/Sn soldering.

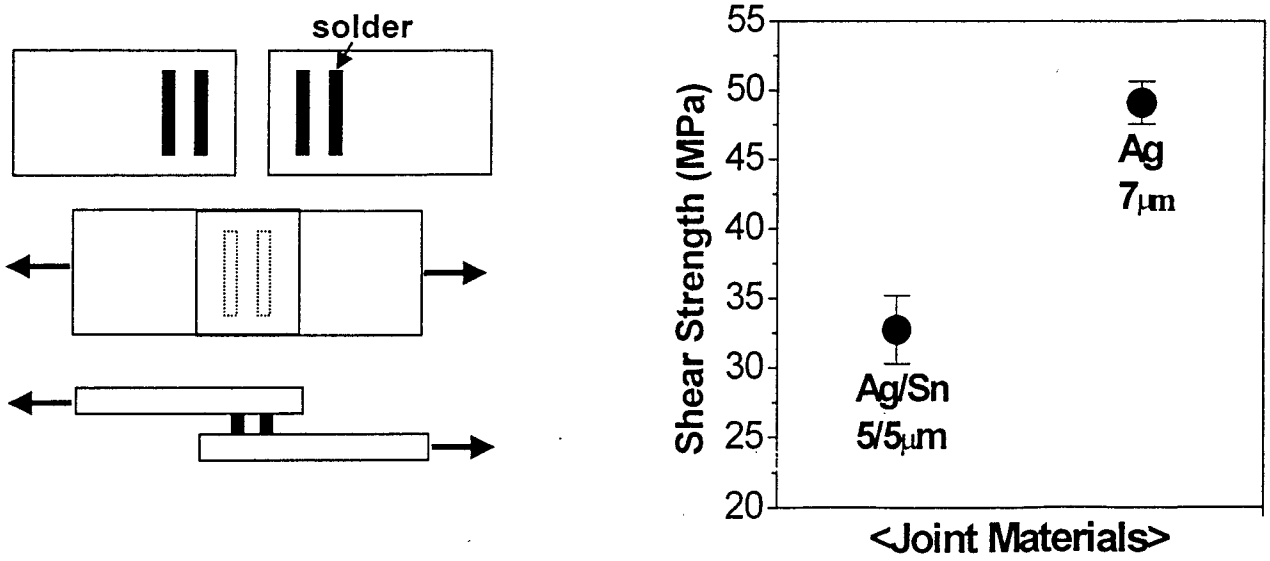


Figure 13 Lap shear test fixture and shear strength for two joint materials

Mechanically separated surfaces of the top and bottom joints were observed by scanning electron microscope. Figure 14 shows that the adhesive failure along the Ag_3Sn/Sn was the most common failure type for the Ag/Sn fluxless soldering joint case. SEM EDX elemental analyses indicated the presence of Ag_3Sn intermetallic compound on the separated surfaces. Figure. 14 also shows the failure the surface of silver joint confirming ductile fracture of the silver itself. The SEM failure surface indicates that the

joint materials rather than joining processes are the cause of observed inferior strength of the fluxless joint of Ag/Sn compared to the high-pressure mechanical joint of silver.

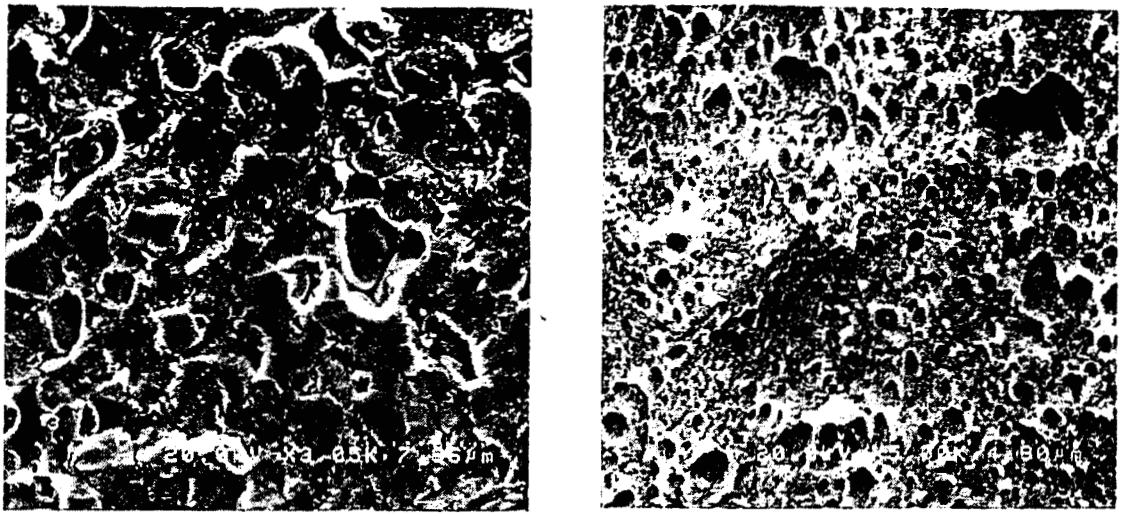


Figure 14 SEM photomicrographs for fluxless and high pressure silver separated by shear test

Reliability

Studies have shown that moisture in the plastic package can cause cracking or delamination during the surface mount process [15]. The SCP, a molded plastic package, can be susceptible to moisture cracking and other plastic reliability concerns. Cracks that propagate through the body of the package or along the lead frame provide a path for ionic contaminants to get to the chip surface, increasing the potential for failure. The CTE mismatch (coefficient of thermal expansion) of the package's materials also creates stress which can cause delamination along the molding compound and lead frame or chip. The influence of moisture on package cracking is discussed below.

Popcorn Cracking Test

Figure 15 shows the moisture absorption behavior of SCP in weight percent. It almost reached the saturation value of 0.09 wt% after 24-hour storage at 85°C /85%RH conditions. Figure 16 exhibits the scanning acoustic tomography (SAT) T-scan images of the SCP before and after 96 hours of moisture absorption followed by two cycles of infrared (IR) reflow. A slight delamination propagation around LOC tape area is apparent for the exposed sample. There was no new delamination interface created due to the moisture induced stress. The SAT and optical microscope inspection results after IR reflow are summarized in Table 6. Neither package crack nor interface delamination was observed, even when the package absorbed moisture for 96 hours. This result demonstrates the excellent resistance of SCP to moisture induced cracking.

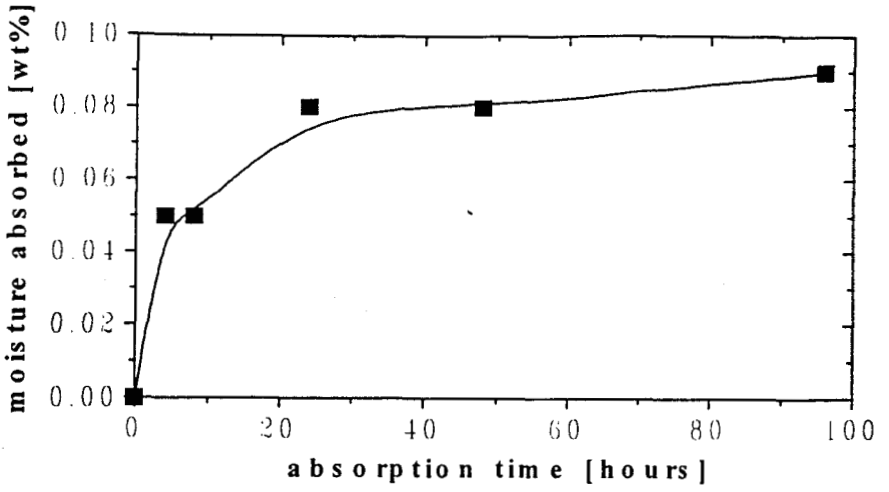


Figure 15 Moisture absorption behavior of SCP

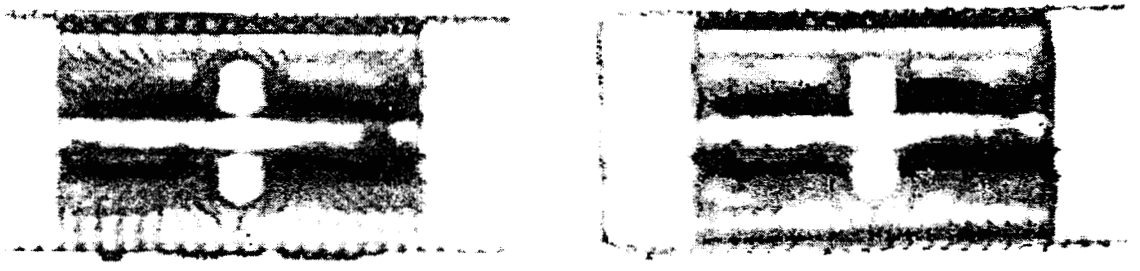


Figure 16 Scanning Accoustic Tomography (SAT) of SCP before and after moisture absorption

Table 6 The moisture induced cracking resistance of SCP

Moisture absorption time (hours)	Crack (failures/sample size)	Delamination (failures/samples size)
4	0/10	0/10
8	0/10	0/10
24	0/10	0/10
48	0/10	0/10
96	0/10	0/10

Temperature Cycle Test and Pressure Cooker Test.

In addition to the moisture induced sensitivity measurement, SCPs were subjected to both temperature cycle and pressure cooker tests. Table 7 shows the test results. Except for a package with Ag/Sn joints,

all other packages survived 200 temperature cycles and 168 hours of the pressure cooker test. These environmental test results indicate that SCP has an excellent reliability, which is comparable to a conventional TSOP plastic package.

Table 7 Electrical test results obtained after temperature cycle test and pressure cooker test

Test Items	Reliability Stress Conditions	Failures/sample size	
		Ag/Sn-Sn/Ag	Ag-Ag
Temp. Cycle Test	-65°C to 150°C, 2 cycles/h 200 cycles	1/16*	0/12
PressureCooker Test	121°C, 2atm, 100% RH 168 hours	0/17	0/12

D2CSP STACK By LG Semicon

The D2CSP is a stack package for 128 Mb SDRAM with two 64 Mb SDRAM in which a bottom leaded package (BLP) was stacked on top of a leaded package. The compliant leaded package permits improvement of the board reliability of the BLP package in the stack form. The D2CSP can be used for high-end application systems, e.g. servers and work stations. In addition, the concept of D2CSP can be extended to accommodate a higher density module with an overall lower cost.

Design and manufacturing process

Figure 17 shows the top and bottom views of a D2CSP for a 128 Mb SDRAM. The lead count is 54 and the lead pitch is 0.5 mm. The top package is a BLP, a CSP for memory package, and bottom has the L-shape leads, called TSOL (thin small outline L). Figure 18 shows a cross-section of a D2CSP and compares the height for three stack types: TSOJ, TSOP, and D2CSP. As noted, the D2CSP is the thinnest package with a height of only 1.85 mm.

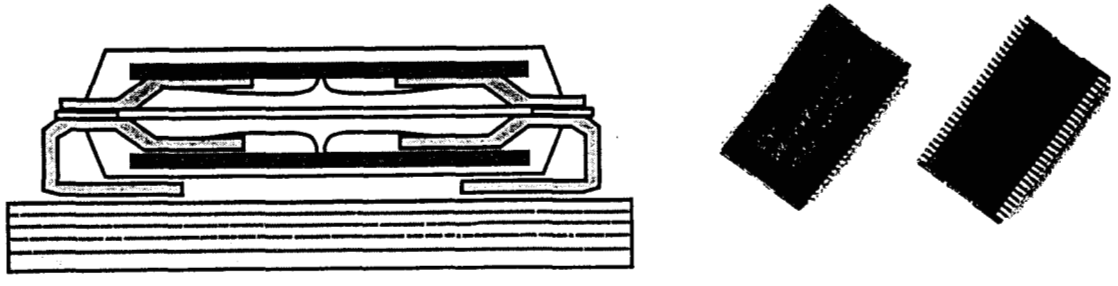


Figure 17 Schematic cross-section and top/bottom photos of D2CSP

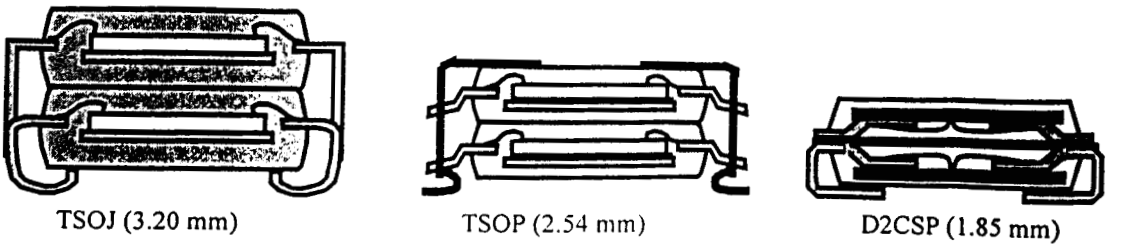


Figure 18 Comparison of 3 different stack technologies

The D2CSP board level assembly processes are basically the same as those for conventional plastic packages as can be observed from the process flow shown in the Figure 19. The package materials are also similar to conventional packages. The stack process uses well-established conventional stencil printing processes which are commonly available and reliable. The 3.5Ag96.5Sn solder paste material was selected for the stencil printing process.

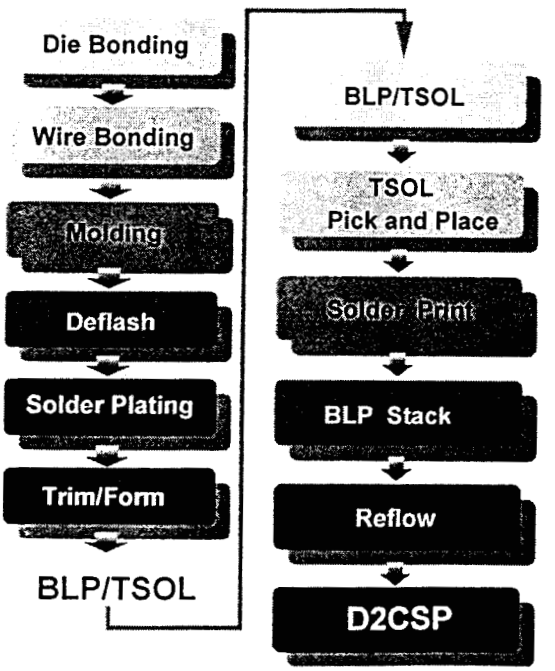
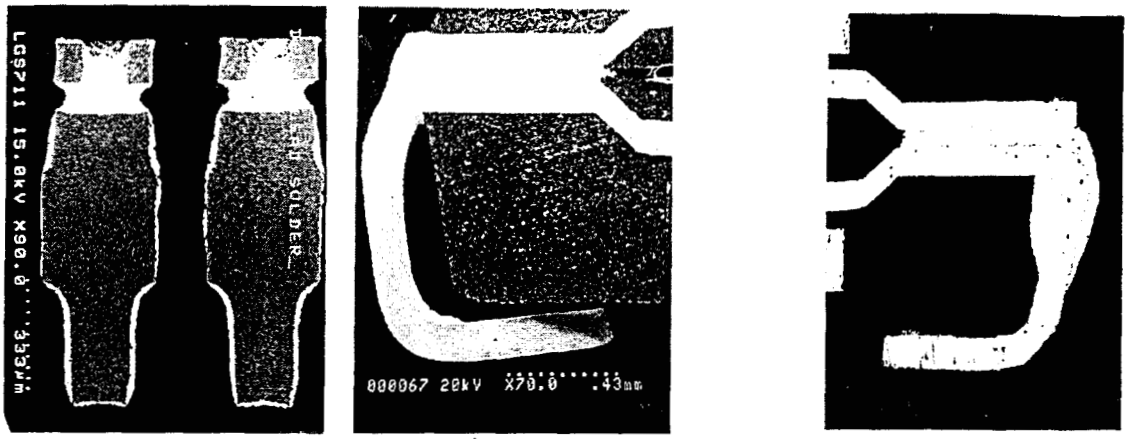


Figure 19 Flow chart for the D2CSP manufacturing process

Figure 20 shows the cross-section of the lead/solder area of a D2CSP after the stacking process. Figure 20 (a), shows the lead end showing a concave solder wetting formation due to the surface tension interaction of solder, lead frame, and epoxy molding compound. The interaction of these surface tensions leads to least occurrence of solder bridging. The gravity effect on the upper package makes the solder volume at the joint uniform, resulting in a controlled package height. The joint thickness between the two packages was measured and found to be between 20 and 30 μm. Figure 20 (b) shows the side view of an unacceptable D2CSP joint. Solder wetted well the gap at the lead end of the BLP package, which led to self-alignment of the BLP on the TSOL, having a good manufacturability for the stack mass production assembly. Since the solder volume was determined by geometry, extra solder tended to

wet the L-shaped leads. It was crucial to control solder volume to minimize solder overflow on the leads of the bottom leaded package. Figure 20 (c) shows a cross-section of a D2CSP with soldered on lead assembled at the initial stage of development. The excessive solder on the leads was found to cause solder bridging after reflow. To prevent bridging, solder volume was optimized by adjusting the stencil opening.



a b c

Figure 20 Solder shape of D2CSP after reflow (a) end view, (b) acceptable solder joint, and (c) unacceptable excessive solder

To check the effect of stacking on package warpage, the U and V displacement fields of a BLP package before and after stacking on a D2CSP as well as after assembly were measured by macroscopic moire interferometry. Moire grating was replicated on the package cross-section and deformation incurred from 100 °C to ambient temperature was determined at room temperature (ΔT = -80 °C).

Figure 21 shows deformation for a BLP before and after stacking. From the U-field deformation pattern, it can be seen that the BLP has a greater compressive strains at its bottom than at its top site . For the V-field, the relative displacement between the center and the package end was measured and found to be about 8.3 μm. This vertical displacement (bending) was attributed to the existance of a larger volume of epoxy molding compound at the package bottom surface.

(a) Before stack (b) after stack

Figure 21 (a) and (b) U and V displacement fields for a BLP before and after stack process, induced by thermal loading of ΔT = - 80 °C, f = 2400 lines/mm

From Figure 21(b), the V-field for a D2CSP, it can be seen that the relative vertical displacement between the center and the board ends are negligible. This is an improvement to the BLP warpage. Therefore, the D2CSP with a lower assembly warpage is expected to be more reliable. Also, note that the relative deformation for the package is symmetric because of the D2CSP structural symmety.

Figure 22 shows moire deformation behavior for a D2CSP assembly indicating low V field displacement between package and PWB. The low deformation indicates that coupling between the package and PWB is small. These results agree well with the results of three-point bend testing (see below). The average shear strain of the leads was difficult to obtain since the U-field lacked an adequate number of fringes to calculate the shear strain. However, the average shear strain was expected to be low because shear terms in the U- and V-fields offset each other. From these results, it can be concluded that the D2CSP should have improved solder joint reliability when compared with BLP package assembly with a higher stiffness and coupling [10].

Figure 22 Moire displacement for D2CSP assembly, (a) U field, and (b) V field displacement, induced by thermal loading of $\Delta T = -80$ °C, f = 2400 lines/mm

Package and assembly reliability

The D2CSP meets the JEDEC level I requirement since it passed preconditioning test (IR reflow test). This means that D2CSP can be stored for a long time prior to SMT assembly without potential of popcorn cracking during reflow process. This high crack resistance stems from the high reliability of the BLP package design. [10]

Board assembly reliability is also important. From a system approach, board reliability and ease of assembly are critical parameters in determining whether to use a new package for an electronics application. System reliability is generally determined by fatigue behavior of solder joints under thermal fluctuation.

Figure 23 shows different aspects of solder joint assemblies of a D2CSP stack: (a) preferred, (b) acceptable, but low in solder, and (c) Pb and Sn phases. Though the joint in (b) showed no signs of cracking, its solder volume needed to be increased to improve joint reliability. From (c), it is apparent that solder materials for the stack package and assembly could reflow together with no effect on the overall of the stack height.

Two hundred twenty two daisy chain D2CSPs were assembled to evaluate the ease of surface mount assembly. The test board had four layers, FR-4, 1.27 mm thick. Solder paste was 63Pb/37Sn eutectic and printed using a 0.15 mm stencil thickness. After solder reflow in a convection oven, all samples

were visually inspected as well as by X-ray. Except for only eight devices failing due to wire bond failure, the rest packages remained in good condition.

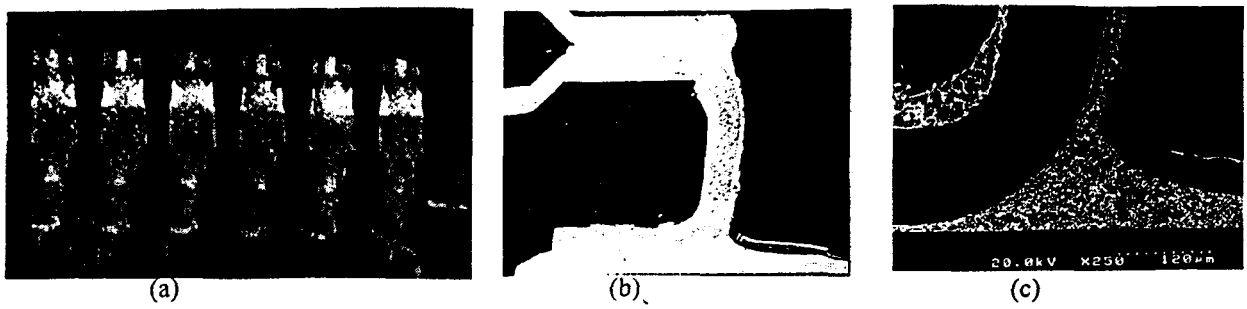


Figure 23 SEM cross sectioanal micrographs for a D2CSP: (a) preferred joints, (b) acceptable, but lower in solder , and (c) microstructure with the Pb (light) and Sn-rich phases

During manufacturing, handling, shipping, rework, etc., the PWB may be subjected to environmental stresses such as bending and twisting. The effects of bending stress on the D2CSP leads and solder joints were addressed by three point bend testing. The test set-up is shown in Figure 24. The load was applied at the center of the test board with a crosshead speed of 3.81 mm/min. The assembly was designed with a daisy chain pattern so that solder failure could be detected by measuring resistance for opens by an ohm-meter. The sample size was 5. Figure 25 shows the load-deflection curves of the test board with and without D2CSP. No solder joint failure was observed even with a load at 4.9 kgf and a deflection at 10 mm. This deflection magnitude is far beyond most manufacturing, handling, shipping, and rework conditions. In addition, from Figure 25, the slope of the two curves was almost the same, meaning the increment of the effective stiffness of the assembly caused by mounting a D2CSP was small.

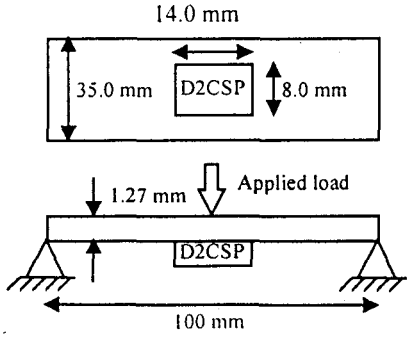


Figure 24 Three-point bend testing on PWB

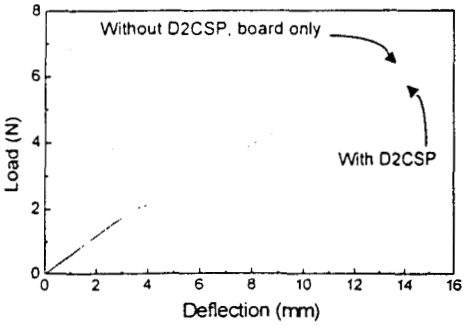


Figure 25 Three-point bending load-deflection curves

Figure 26 shows the joint failure during three-point bend testing. The joints between the package and PWB were cracked, while there were no cracks at the joints between the two stacking packages. Thus, it was concluded that the compliant L-shape leads of D2CSP absorbs most of the strain during bending, and that is why there was little difference between the two curves in Figure 25.

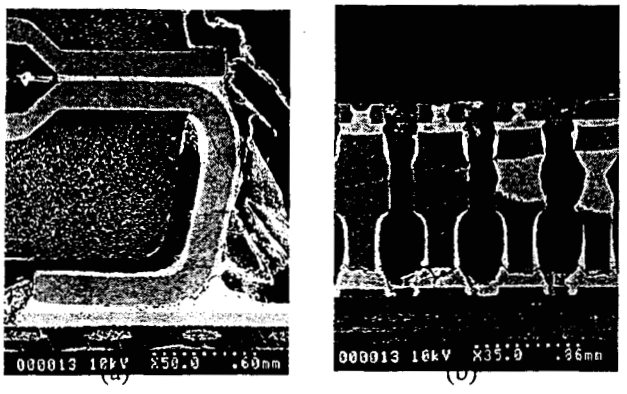


Figure 26 Solder joint failure due to three-point bending, cross-section (a) and end view (b)

Accelerated thermal cycling test was performed to check the solder joint reliability. The test condition was –65 to 125 °C, 2 cycles per hour. The solder joint failure criterion was 20 % resistance increase. Assemblies survived 1,500 cycles with no failures.

Rework

Rework for the stack packaging technology is challenging since it involves reflows of at least two competitive solder joints. As the stack becomes more complex, the cost of rework increases. For D2CSP conventional methods can be used since the package assembled on the board is a conventional leaded package. Reasons for rework may include: (1) removal of solder manufacturing defective including bridges, missing or defective solder balls, and insufficient solder volume, and (2) remove of a defective package, BLP, or TSOL, and its replacement with a functional one

Figure 27 shows a rework set up that was used to successfully rework a D2CSP. Packages showed no signs of cracking and delamination after rework.

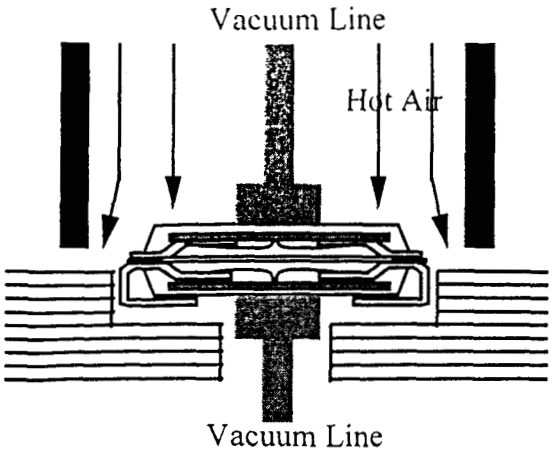


Figure 27 D2CSP rework system

Applications

Because of its miniaturized size, high producibility, high reliability, and high density, the D2CSP can be used for high-end systems such as work stations and servers. The concept of D2CSP can be applied to other stack packaging such as 256 Mb SDRAM, and 512 Mb SDRAM. The cost of this stack memory will be very low compared to their single unit configuration. However, there are technical issues including thermal and electrical, that need to be resolved before full implementation of high density stack modules.

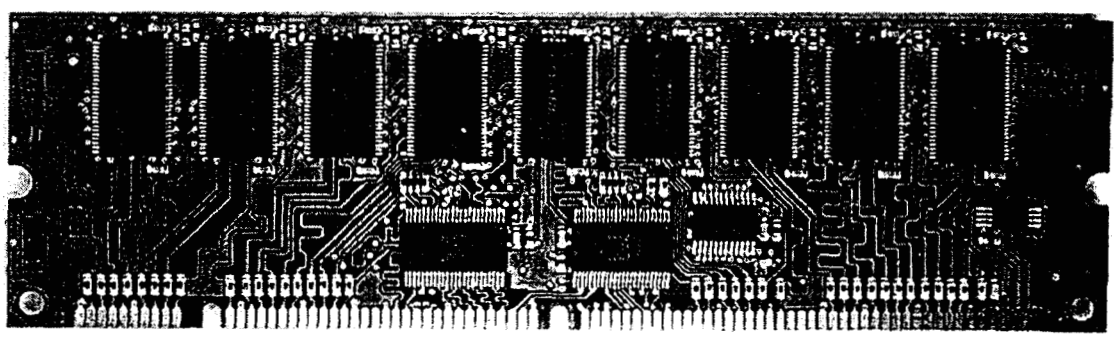


Figure 28 The application of the D2CSP: registered DIMM of with memory size of 256 MB

NEC's Three Dimensional Memory Module (3DM)

Area array stack memory developed by NEC has flip chip die on interposer with additional large peripheral solder bumps for interstack interconnection. Figure 29 depicts a four module configuration. This package has four times the memory of a conventional TSOP and has a slightly larger foot print. One type of first-level interconnection is a gold stud bump which is a joint by forming thermal compression. Even though these bumps do not require solder and flux, they require a high temperature ceramic substrate to surviving the high temperature bonding process. In another type, a solder bump with a lower reflow temperature requirement (instead of a stud bump) was used to reduce the memory exposure to elevated temperature during solder reflow. In addition, copper core ball bumps were used for the peripheral interconnections, in order to control stack space and avoid PWB contact to die. Similarly to other flip chips, dies were underfilled to enhance first-level reliability interconnection.

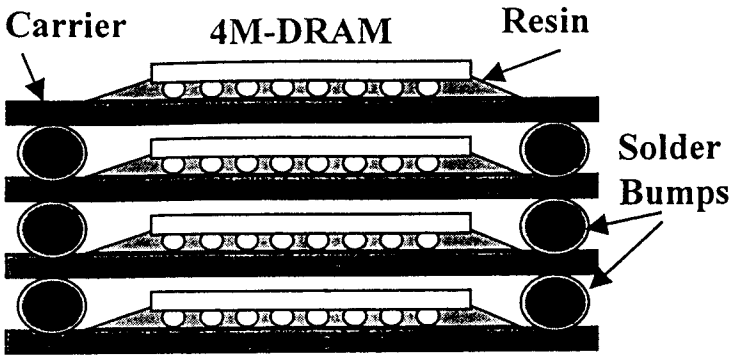


Figure 29 NEC 3D Memory Module, 4 packages

Reliability tests were performed on single as well as 3D modules with different die sizes [11]. Table 8 lists characteristics of these modules and Table 9 tabulates the environmental test results. The tests performed included: heat test (HT) at 125°C, thermal cycle test (T/C) in the range of –40°C to 125°C with 30 minute cycle duration, and a pressure cooker test (PCT) at 110°C, 85% humidity, in a 1.2 atm. For the smallest die size, environmental behavior of the single and 3D modules were the same. This was not true for the larger dies. For the modules with the larger dies, the 3D version had inferior thermal cycling behavior. The single module survived 750 T/C whereas the 3D version showed signs of failure at 100 cycles with the majority of module failures at 500 cycles. It was determined that the weakest link was indeed the peripheral inter stack interconnection. Peripheral balls have the largest distance to neutral point (DNP) and therefore maximum CTE mismatch strains.

The second level solder joint reliability for the small die module was evaluated by assembly on DIMM epoxy board, similar to inter die substrates. These were subjected to 3,000 thermal cycles. There were no solder joint failure of any interconnection, i.e., between dies, peripheral inter stack interconnections, or solder joints on DIMM. It was concluded that high reliability of system interconnection is possible.

Table 8 Characteristics of NEC single, double, 3D modules

Type	1	2	3
Type of Chip	16Mb	64Mb	64Mb (shrunk type)
Die Size	5.9X10.75X0.28	8.53X18.8X0.32	7.13X13.95X0.32
Substrate Size	9.2X17.3X0.3	14.5X20.4X0.5	13.4X16.0X0.5
Module Height	2.6	1.9	1.9
DIMM Board	21.8X133.35X1.27mm		

Table 9 Reliability of single and 3D memory modules

Type	Sample Form	Test Item	Result		
1	Single	HT,PCT T/C	2000H or cycles OK		
	3D	HT,PCT T/C			
2	Single	HT, PCT T/C	750H or cycles OK		
	3D	HT,PCT			
		T/C	300cyc NG (86%)	500cyc NG (84%)	750cyc NG (100%)

MCM version of this technology on ceramic substrate was used for a RISC (reduce instruction set computer) for application in a high performance workstation. The design consists of a D/L (deposited organic thin film on laminated printed-circuit board) base substrate, a glass ceramic based organic thin film multilayer build up CSP and a 3Dimentional glass ceramic memory module. This package is in its prototype stage and is being considered to be used for various workstation and supercomputer applications.

Area Array Stack Memory by Micron

Micron Technology Inc. has considered several stacking technologies for DRAM. A stackable fine pitch area arrays (SBGA), similar to the NEC stacking, is one of this approach as shown in Figure 30.

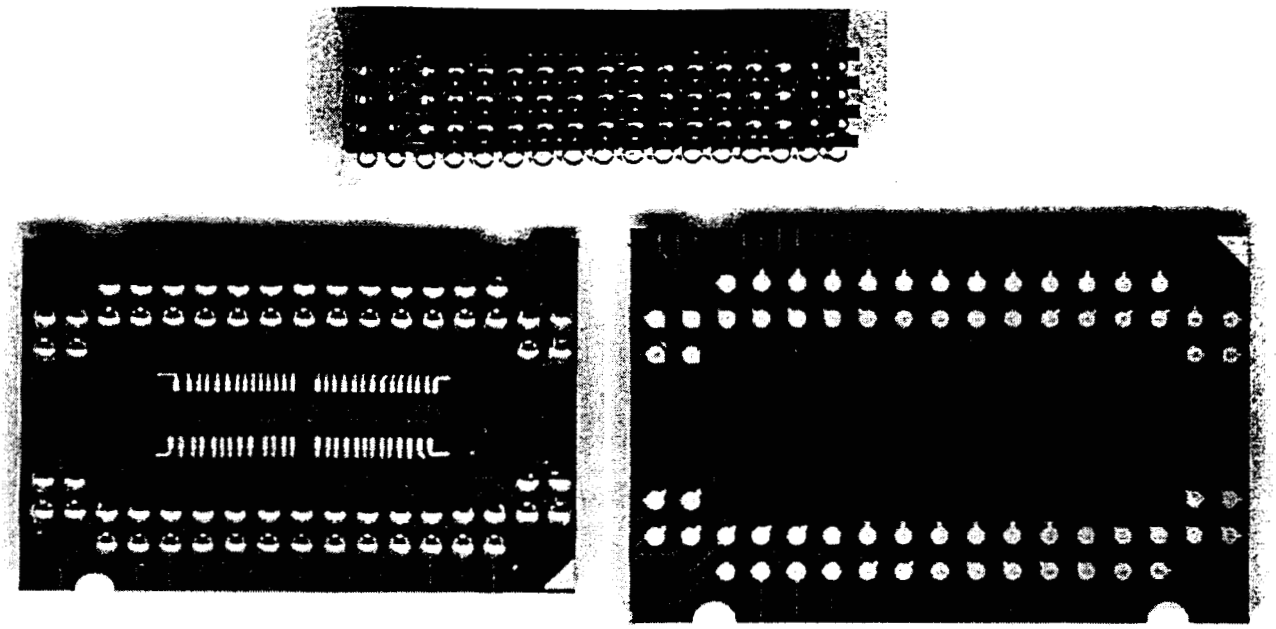


Figure 30 4D stack memory design by Micron

An SBGA is the stacking of one array upon another. The stackable FBGA package is configured such that conductive elements are placed along the outside perimeter of a semiconductor device (integrated circuit (IC) device) mounted to the SBGA. The conductive elements also are of sufficient size so that they extend beyond the bottom or top surface of the IC device. Wire interconnects connect the IC device in a way that does not increase the overall profile of the package. Encapsulating material protects both the IC device and the wire interconnect, as the conductive elements make contact with the SBGA positioned below or above to form a stack. A memory chip is mounted upon a first surface of a printed circuit board substrate forming part of the SBGA. Lead wires, or bump interconnects, are used to attach the IC device to the printed board substrate and encapsulant is used to contain the interconnect within and below the matrix and profile of the conductive elements.

Additionally, certain pins on the SBGA in the stack require an isolated connection to the PC board. An example of such a requirement is when an activation signal for a particular IC device within the stack must be sent solely to that device and not to any of the other devices within the stack. This isolated connection connects to an adjacent ball on a different FBGA stack above or below that particular isolated connections. In common pin layouts of devices stacked together, each device requires an isolated connection to the PC board.

This provides for a stair step connection from the bottom of the FBGA stacked array to the top that allows each device, from the bottom one to the top one, to have an isolated connection from each other.

This allows IC devices to be stacked one upon each other while maintaining a unique pin out for each pin required in the stack.

Fujitsu Stacked MCP (Multi-Chip Package)

Fujitsu's MCP uses stacked die as shown in Figure 31. The Stacked MCP (Fine Pitch BGA) has the following characteristics:

- Package is FPBGA with 8x8 (56 balls, excluding non-connected balls), 0.8 mm pitch
- It requires 30% less board space than two separate TSOPs
- Stack can be configured to have Flash and SRAM combination of 8x8, 8x16, and 16x16 bit memory
- Flash and SRAM memory can extend up to 128 Mb for the same package pin configuration

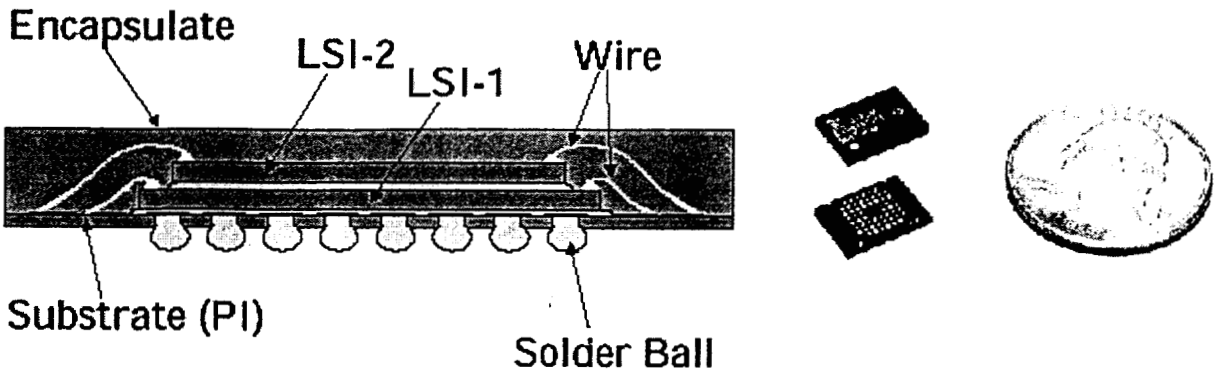


Figure 31 Fujitsu's Multi-Chip Package

Table 10 compares applications of MCP for flash and SRAM. Currently, there is an active proposal on registration for a Low Profile Fine Pitch (FBGA) Stack MCP family[7]. Figure 32 shows the proposed package configuration for inclusion in the MCP specification.

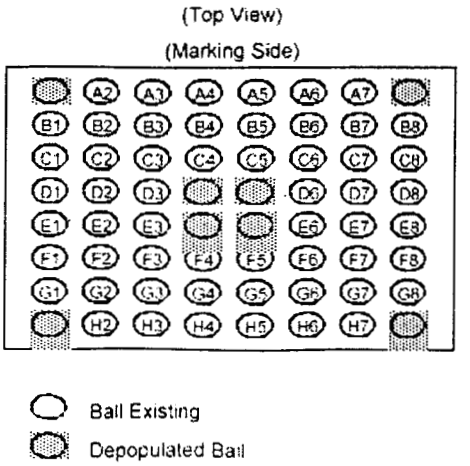


Figure 32 Pin layout of SRAM is adjust to that of Flash memory including I/O, power, and ground

Table 10 Application of MCP for Flash and SRAM

Combination of Flash and SRAM

Flash \ SRAM	1Mb	2Mb	4Mb	8Mb
8Mb	√	√	√	√
16Mb	√	√	√	√
32Mb	√	√	√	√
64Mb	√	√	√	√
128Mb	√	√	√	√

These MCPs can be used both configurations of x8 and x8/x16.

The density of SRAM can be extended to 128Mb

Array and Pitch

1. Array 8x8
2. Pitch 0.80mm(typ.)

REFERENCES

1. Al-sarawi, S. F., *et al.*, "A Review of 3D Packaging Technology," *IEEE Trans-CPMT-B*, Vol 21, No. 1 (1998), pp. 2-14.
2. Alkalai, L., "Advanced Packaging Tecnologies used in NASA's 3D Space Flight Computer," Proceedings on High Density Packaging and MCMS/IMAPS, Denver, Apr 6-9, 1999, pp 85-90
3. Hunter, D., Integrated Avionics System (IAS), Integrating 3-D Technology on a Spacecraft Panel," Proceedings on High Density Packaging and MCMS/IMAPS, Denver, Apr 6-9, 1999, pp 80-84
4. Staktech in electronic- Cady, J. Bustami, T., "3-D Packaging helps Solve Computer Memory Problems," Electronics Packaging & Production, Feb. 1996
5. Choi, K-w, et al, " Development of 128 DRAM by Stacked Packaging Tecnology," Proceedings of 3D Packaging Advanced Technology Workshop, Oct. 13, 1997
6. Hamano, T., et al, "SOC Package and 3D-Package Module for Memory Device," Proceedings of the IMAPS ATW on Chip Scale Packaging, Austin, Tex., August 1997
7. Hamano, T., JEDEC, JC 11 proposal, "Common Specification Flash Memory and Static RAM in Stacked, private communications
8. Cho, S-J, et al, "A Novel Robut and Low Cost Chips Package," private communications
9. Choi, K-S, et al, "D2CSP (Double Density CSP): A New Solution for High-Density Packaging," 49th IEEE/CPMT, 1999
10. Choi, K-S, et al, "Solder Joint Reliability of the BLP Package," Proceedings IPC/SMTA Electronics Assembly Expo, Rhode Island, Oct. 1998
11. Kyougku, Y., et al, "3-Dimensional Memory Module Assembly Technology," IEMT/IMC Proceedings, 1998, pp 272-277
12. Takahashi, N., et al, "3-Dimensional Memory Module," 1996 Electronic Components and Technology Conference, pp113-119
13. Wood, A., Wark, J., Micron Technology, Inc., private communications
14. Oguchi, S., et al, "Sealed Stack Arrangement of Semiconductor Devices," US Patent No. 5701031
15. Rymazewski,E., et al., Microelectronics Packaging Handbook, Chapman & Hall, 1997

ACKNOWLEDGMENTS

The review described in this publication was supported by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge contributions of the following individuals which shared their recent research activities for inclusion in this chapter. These are Don Hunter, JPL, Kwang-Sung Choi, LG Semicon, Deok Hoon Kim and Soon-Jin Cho, Hyundai, James Cady, Staktek, and Alan Wood and James Wark, Micron. Also, thanks to Young Gon Kim and Joe Fjelstad, Tessera, for their information gathering initiation and support.